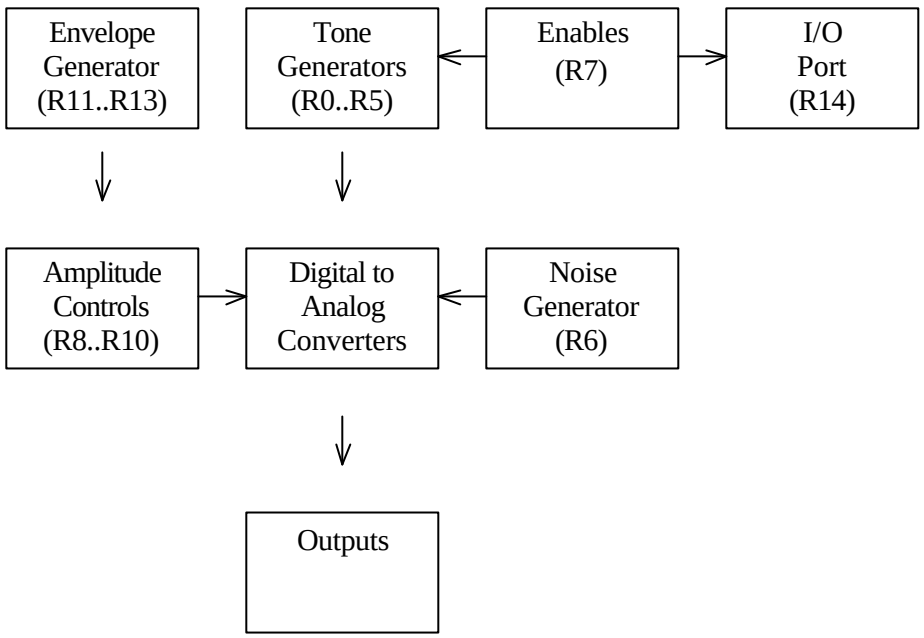
Appendix IX
The Programmable Sound Generator.

The programmable sound generator (PSG) is an AY-3-8912 chip. This is briefly described in section 7.1. The PSG has a number of registers which are described below. This information is provided for the interest of the user, particularly if hardware enveloping is to be used (in which case section (e) will be of special interest). However, the software enveloping provided by the Sound Manager can achieve all that the sound chip is capable of unless very short attacks or decays are required.

If the user is intending to drive the sound chip directly rather than by using the Sound Manager then the information presented is not complete and the user should consult the manufacturer's data sheet. The user is advised to call the routine MC SOUND REGISTER to write data to a sound chip register as this obeys the timing constraints on access to the sound chip.

The following diagram indicates the interactions between the various sections of the sound chip:



The sound chip data registers are as follows:

Register 0:	Channel A tone period fine tune.
Register 1:	Channel A tone period coarse tune.
Register 2:	Channel B tone period fine tune.
Register 3:	Channel B tone period coarse tune.
Register 4:	Channel C tone period fine tune.
Register 5:	Channel C tone period coarse tune.
Register 6:	Noise period.
Register 7:	Enables and I/O direction.
Register 8:	Channel A amplitude and envelope enable.
Register 9:	Channel B amplitude and envelope enable.
Register 10:	Channel C amplitude and envelope enable.
Register 11:	Envelope period fine tune.
Register 12:	Envelope period coarse tune.
Register 13:	Envelope shape
Register 14:	Input from or output to port A.
Register 15:	Not used.

a. Tone Generators (Registers 0..5)

Each channel has two tone period registers associated with it. These set the period of the sound to be generated (in units of 8 microseconds) by that channel. The fine tune register stores the least significant 8 bits of the period; the coarse tune register stores the most significant 4 bits of the period. To include the tone in the output of a channel the appropriate bit in the enables register must be cleared.

b. Noise Generator (Register 6).

There is a single pseudo-random noise source. The output from this can be included in the output of any of the three channels (as specified by the enables register). The period of the noise generator is set by bits 0..4 of the noise period register. The period specifies the middle frequency of the noise produced in 8 microsecond units.

c. Enables (Register 7).

The enables register specifies whether tone or noise is to be included in the output from each channel. It also specifies whether the I/0 port is to act in input or in output mo de. The bits are allocated as follows:

Bit 0:	Channel A tone disable.
Bit 1	Channel B tone disable.
Bit 2	Channel C tone disable.
Bit 3	Channel A noise disable.
Bit 4	Channel B noise disable.
Bit 5	Channel C noise disable.
Bit 6	Port A output mode
Bit 7	Not used.

Note that port A is connected to the keyboard and joystick and so the port must always be in input mode. The user must ensure that bit 6 of the enables register is always set to zero.

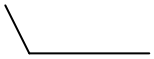
d. Amplitude Controls (Registers 8-10).

Each channel has an amplitude control register associated with it. Bit 4 of this register specifies whether hardware enveloping is to be used for the channel. If the bit is set then the channel amplitude (volume) is under the control of the hardware envelope generator. If the bit is clear then the amplitude is set by bits 0..3 of the register - a value of 0 means no sound and a value of 15 means maximum volume.

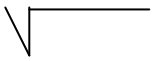
e. Envelope generator (Registers 11-13).

The sound chip has a single hardware envelope generator which can be used to control any combination of the three sound channels as specified by the channel's amplitude register (see (d) above). Bits 0 to 3 of register 13 control the shape of the envelope in a rather unobvious manner. The following table gives values required to generate each of the 8 hardware envelopes that are possible. Other values (0..7) duplicate envelopes 9 and 15.

8:  Repeated jump up and ramp down.

9:  Jump up and ramp down once then hold at minimum volume (zero).

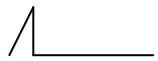
10:  Jump up then repeatedly ramp down and up again.

11:  Jump up and ramp down then jump up and hold at maximum volume (fifteen).

12:  Repeatedly ramp up and drop down.

13:  Ramp up then hold at maximum volume (fifteen)

14:  Repeatedly ramp up and down again.

15:  Ramp up and drop down once then hold at minimum volume (zero).

The length of each of the ramps, upwards or downwards, is set by the envelope period. The envelope period is a full 16 bit value whose less significant byte is stored in register 11 and whose more significant byte is stored in register 12. The period is given in 128 microsecond units and is the time between steps in the ramp. Since the ramp has 16 steps (corresponding to the 16 volume settings) the total time taken for the ramp is the envelope period times 1024 microseconds (i.e. the envelope period approximately sets the total time for the ramp in milliseconds).

f. I/O Port (Register 14).

The mode of operation of the PSG port is set by a bit in the enables register (see section (c) above). However, since port A is dedicated to reading the keyboard and joysticks it should always be operated in input mode. The port may be read by reading the contents of register 14. However, scanning the keyboard is a complex action and is best left to the Key Manager which provides ample facilities for access to the keys.

References to port B in the manufacturer's data sheet should be ignored as the AY-3-8912 is a version of the chip that does not have port B.