

Video

DIGITALISER

- ★ Resolution 312 x 255
- ★ 8-bit Luminance Resolution
- ★ Controller Board to detect Line & Sync Pulses Available

by Mark Brighton and
Robert Kirsch

A Video Digitiser is a device which converts a video picture, such as the output of a video camera or V.C.R. (still frame) into digital words representing the luminance or brightness of coordinates (X, Y) within the picture. Thus, by sampling and converting all coordinates in turn, a stream of digital words representing the video picture may be sent to a host microcomputer and displayed on a graphics screen, or stored on disk or tape.

The resolution of the final computer picture will depend on the graphic capability of the host computer, up to the limits of the Digitiser.

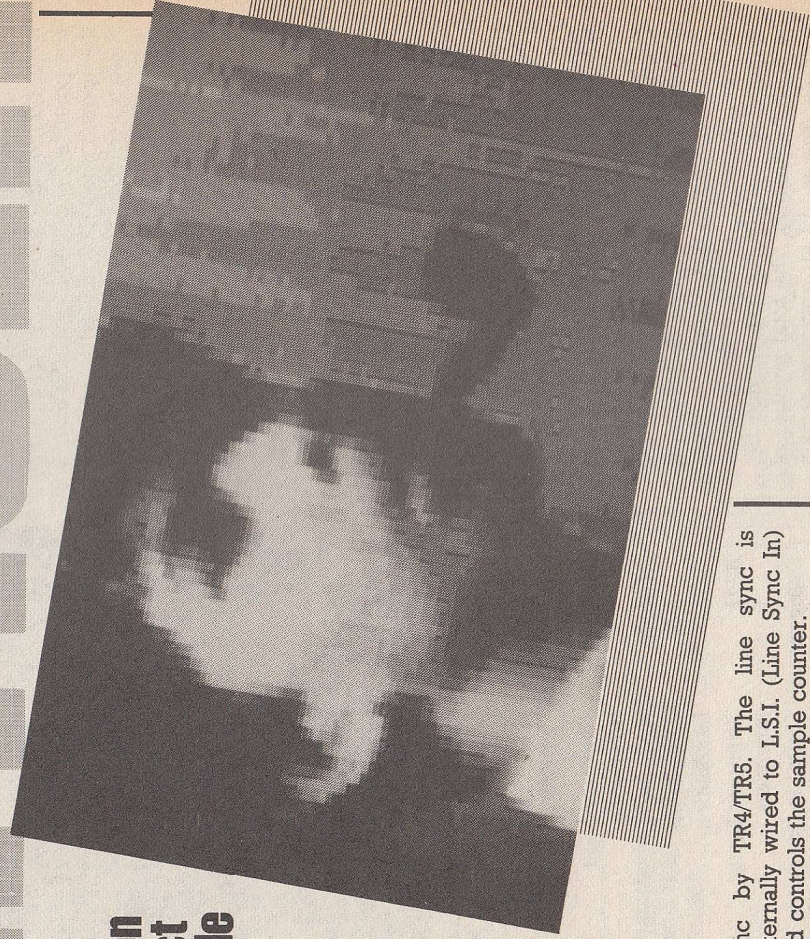
In this case, the maximum vertical resolution of the Digitiser is the same as the number of complete lines in a video frame, i.e. 312 (although twice this number should be available if the interface frame is also stored).

The horizontal resolution is 255 which is the possible number of sample points in one line scan, although some of these will be in non-valid picture area.

The resolution of the luminance samples is 8-bit for a standard video level, ≈ 1 volt of video. Most microcomputers will not be able to combine these resolutions in a graphic screen, and a compromise between (X, Y) resolution and luminance resolution will have to be made when programming.

Circuit Description

In Figure 1, the video content of the incoming signal is stripped off by TR1 to leave composite sync, which is further split into frame sync by TR2/TR3 and line



sync by TR4/TR5. The line sync is externally wired to L.S.I. (Line Sync In) and controls the sample counter.

The sample counter (IC3,4) is preset by an incoming line sync pulse inverted by IC2b, a position byte having been set up on DP0-7 by an 8-bit output port from the host computer.

The line sync pulse also clocks flip-flop IC5 via OR gate IC6d, setting IC5 output high and enabling the oscillator IC1b via IC1c, which is used as a Schmitt Inverter.

This oscillator clocks the sample counter at a frequency determined by RV1/C4 (≈ 4 MHz) and causes it to count down to zero and carry, disabling the oscillator by resetting IC5 via IC6d to prevent any further sample pulses during the present line.

The carry pulse is inverted by IC2c, and charges C9 which then discharges through R2, lengthening the pulse inverted by IC2a to operate the analogue switch IC8. This connects DC restored video from C25/D2 to the hold capacitor C8, which charges to the video voltage. The lengthened carry pulse is also

inverted by IC2f whose output goes to the 'Start of Conversion' input on the analogue to digital converter IC10. When the pulse ends, the analogue switch opens and the 'Hold' video voltage is applied to IC10 via IC9, a high input impedance op-amp connected as a voltage follower, i.e. unity gain.

The End Of Conversion (EOC) output from IC10 goes low enabling the clock oscillator IC1d via an emitter follower TR6 and IC1a which is connected as a Schmitt Inverter. After the ninth cycle of the oscillator, the EOC output of IC10 goes high, disabling IC1d and indicating end of conversion. This signal is sent to the host computer, indicating that the output of the A/D converter is valid. The host computer reads and stores the data on P(DA) via an 'X' bit input port, where 'X' is the required number of luminance bits.

IC7 is a voltage converter which produces a -5 Volt supply for IC9 and IC10.

Construction

Referring to the Parts List and PCB layout diagram (Figure 2), insert and solder veropins 1 to 6 from the underside of the board (Side 1) and fit Link 1 if termination of the video signal is required. Insert and solder in position all resistors, capacitors and diodes, taking note of polarity.

Insert and solder all IC sockets, transistors, BR1 and mount REG1 using the insulating washer and heatsink supplied, first smearing mating surfaces with heat transfer compound (not supplied).

Double check your work for short circuits, components in wrong places, etc. Five minutes careful examination of your work now may save much time and expense later.

Plug IC7 into its socket, ensuring correct orientation.

Testing

Minimum system I/O requirement is one 8-bit output port and one 8-bit input port. This allows for up to 5 bits of luminance information, which should be

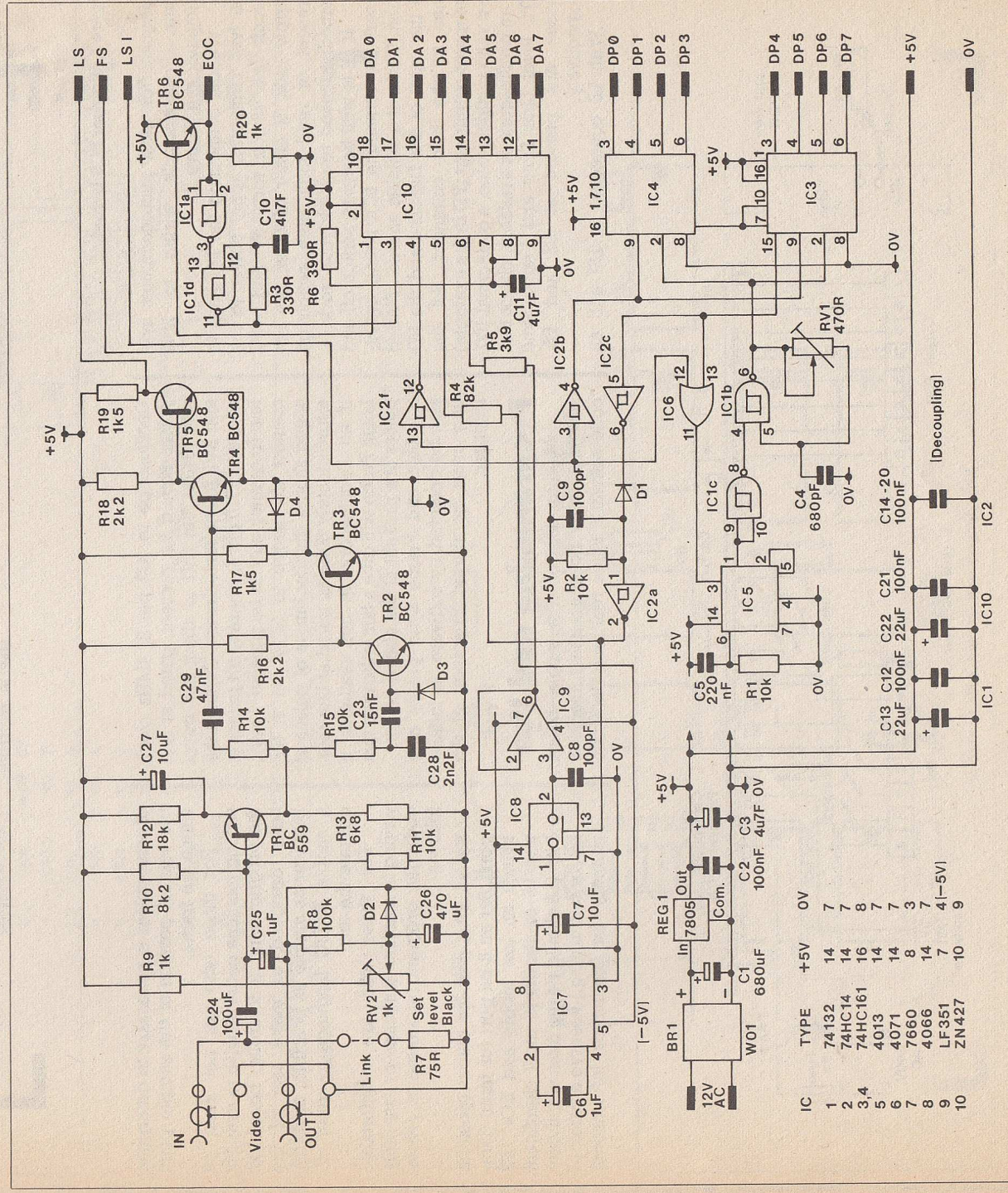
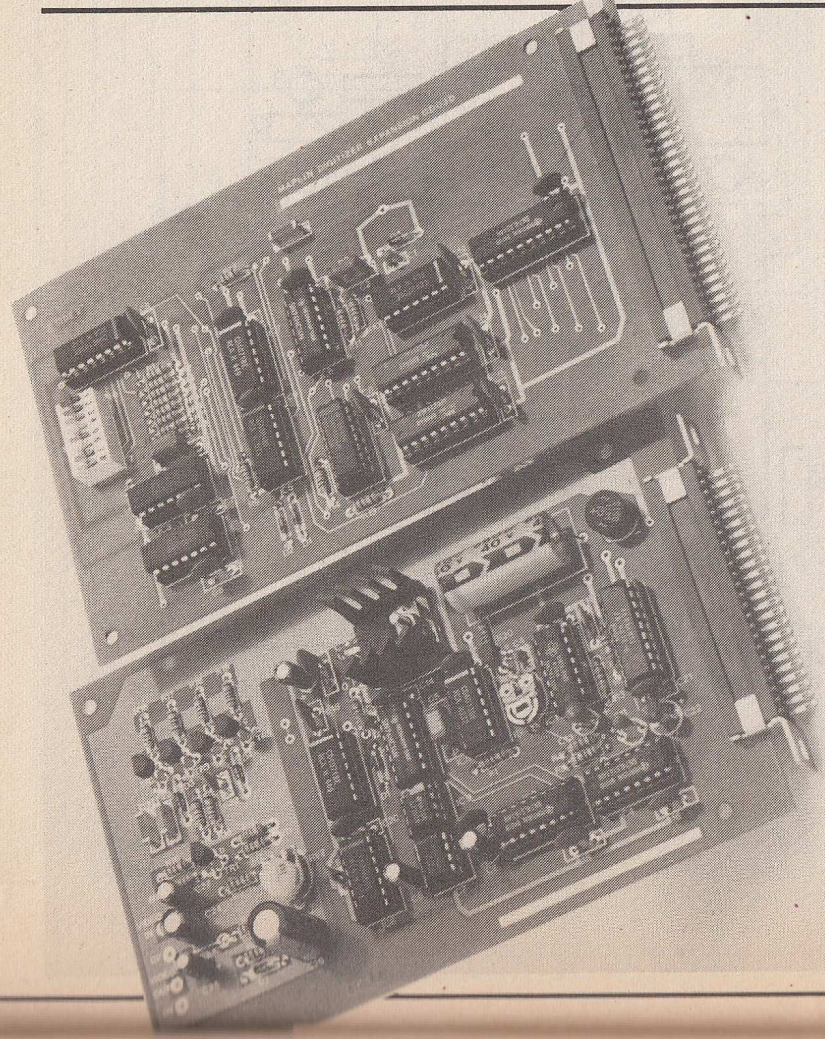


Figure 1. Digitiser Circuit
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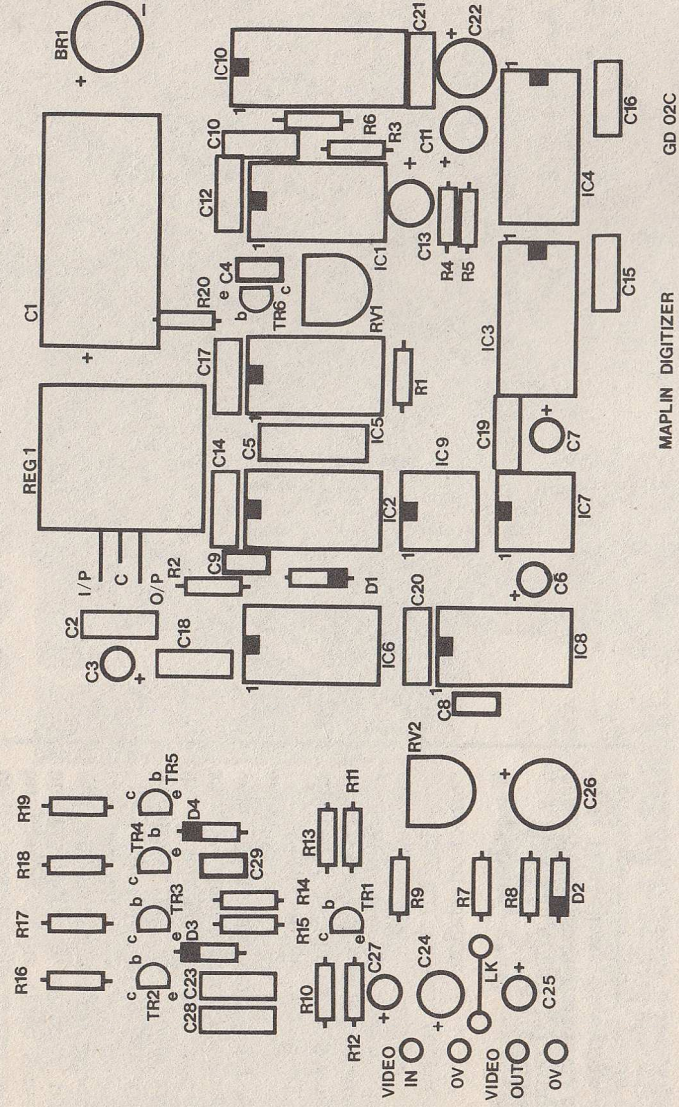


Figure 2. Digitiser PCB Layout

adequate for most microcomputer systems. For example wiring to host computer see Figure 3.

Without connecting the I/O lines to the host computer, apply power to the circuit and check for +5V and -5V supply rails. If either of these are not present, or read high, then switch off immediately and re-check your work.

If all is well however, switch off and insert the remaining IC's noting orientation. Connect a suitable source of video to the input of the Digitiser and the I/O computer output port (PD in the example) to a valid position value, e.g. decimal 100. If an oscilloscope is available, check that TTL level Line Sync and Frame Sync pulses are present at LS and FS, respectively.

With LS connected to LSI and an

Oscilloscope to IC3 pin 2, 4MHz clock pulses should be present, gated at line rate (64µs). Set RV1 to about half travel and RV2 fully anticlockwise. Connect the scope to IC10 pin 4, where short pulses at line frequency should be present. Lastly, connect the scope to IC10 pin 3; the scope should display bursts of pulses at approximately 600kHz, gated at line rate. If an Oscilloscope is not available, a Logic Probe will give a fair indication that pulses are present at the above points.

Line and Frame Sync pulses may also be detected by software, as indeed they must be during operation of the Digitiser.

Programming and Use

Making use of this single board system is only possible using machine code software, since real time detection

of sync pulses is necessary to determine the vertical position of the sample point within the frame.

For those who are not keen on writing machine code, or wish to simplify the programming, a controller board has been designed to make use of the Digitiser as simple as possible, enabling a simple BASIC language program to operate the unit.

For those who are comfortable writing in machine language or assembly code, the program requirements are as follows:-

1. Set an 8-bit port for output (position port). Set an 8-bit port for input (luminance on low nibble and EOC, FS and LS on the three most significant bits. (LS should be the most significant bit for fast testing.) Reserve a block of memory for luminance information,

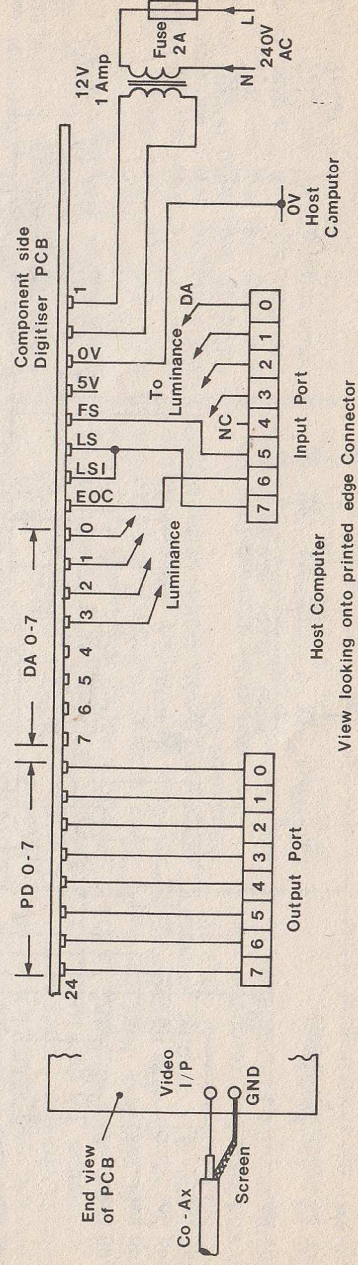


Figure 3. Board System Wiring

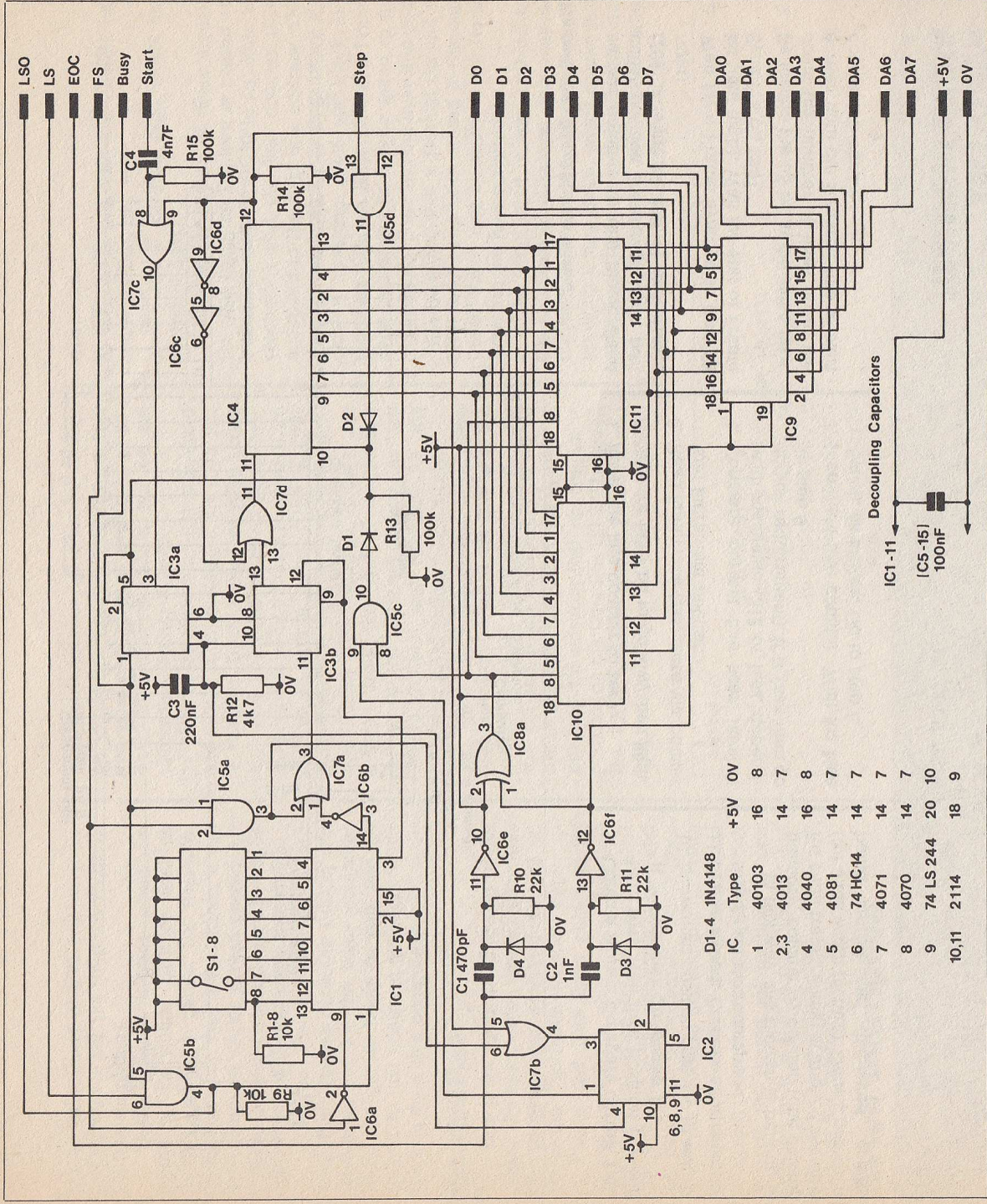


Figure 4. Controller Circuit

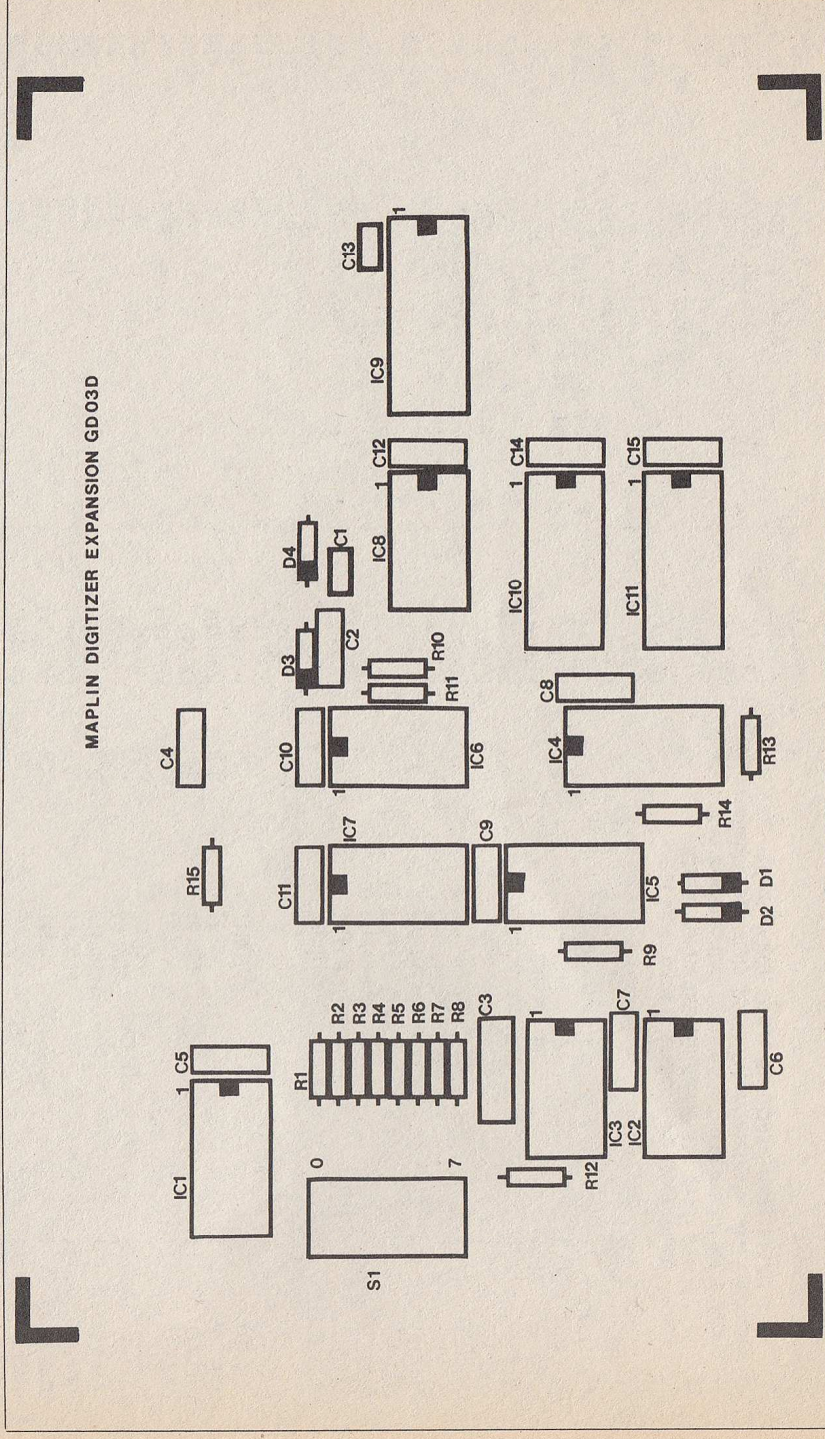


Figure 5. Controller PCB Layout
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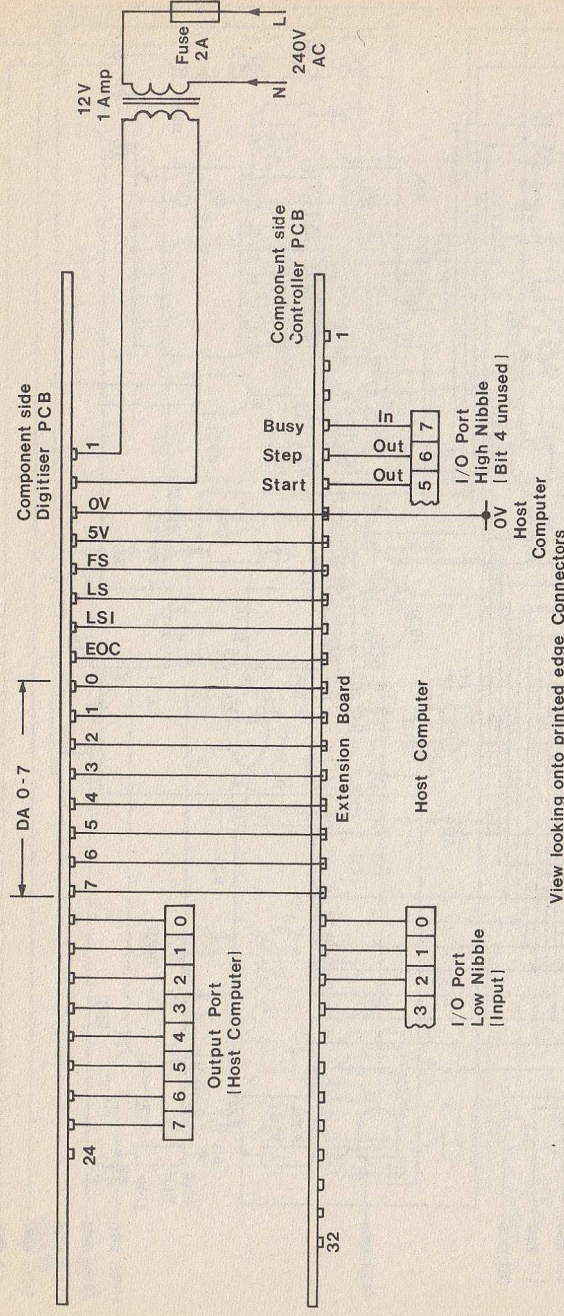


Figure 6. Two Board System Wiring

set up pointers to this block. Send initial position byte to position port (254 is extreme left, 0 is extreme right).

2. Wait for a Frame Sync pulse (test FS bit until high). Wait for end of Frame Sync (FS bit low).
3. By testing the LS bit in the same way, count the number of lines down the screen until the required line to start conversion occurs.

4. Reset the line counter to zero.
5. Wait for EOC bit to go low, then high.
6. Read luminance bits, store via pointer and increment pointer.
7. Compare current line scan number with maximum (312 or less, depending on requirement). If \geq max then go to step 9.
8. Increment line counter. Wait for Line Synch. as before. Go to step 5.

9. Column stored. Compare current position byte with final position number. If \geq max then go to step 11.
10. Increment position port. Go to step 2.
11. Frame stored. Process information to display on microcomputer.

In this way, the picture is built up in memory, column by column (one column for each frame, 20ms) in about 5 seconds (for a full width picture). Once a picture is being stored and displayed, contin-

VIDEO DIGITISER PARTS LIST

RESISTORS: All 0.6W 1% Metal Film

R1,2,11,14,15	10k
R3	330R
R4	82k
R5	3k9
R6	390R
R7	75R
R8	100k
R9,20	1k
R12	18k
R13	6k8
R16,18	2k2
R17,19	1k5
R10	8k2
RV1	470R Hor Sub-Min Preset
RV2	1k Hor Sub-Min Preset

CAPACITORS

C1	880 μ F 40V Axial Electrolytic
C2,12,14-21	100nF Mintidisc
C3	4 μ 7F 63V P.C. Electrolytic
C4	880pF Ceramic
C5	220nF Poly Layer
C6,26	1 μ F 100V P.C. Electrolytic
C7,27	10 μ F 50V P.C. Electrolytic
C8,9	100pF Ceramic
C10	4n7F Poly Layer
C11	4 μ 7F 16V Tantulum
C13,22	22 μ F 16V Tantulum
C23	15nF Poly Layer
C24	100 μ F 10V P.C. Electrolytic
C26	470 μ F 16V P.C. Electrolytic
C28	2n2F Poly Layer
C29	47nF Mintidisc

SEMICONDUCTORS

DA-D4	IN4148	4	(QL80B)
TR1	BC559	1	(QQ18U)
TR2,3,4,5,6	BC548	5	(QB73Q)
BR1	W01	1	(QL38R)
REG1	LA7805UC	1	(QL31J)
IC1	74132	1	(WH03D)
IC2	74HC14	1	(UB10L)
IC3,4	74HC161	2	(UB41U)
IC5	4013BE	1	(QX07H)
IC6	4071BE	1	(QW43W)
IC7	7680	1	(Y775S)
IC8	4066RE	1	(QX23A)
IC9	LF351	1	(WQ30H)
IC10	ZN427	1	(UF40T)

MISCELLANEOUS

Digitiser PCB	1	(GD02C)
Vaned Heatsink	1	(FL68N)
Kt (P) Plus	1	(WR23A)
DIL Socket 8-Pin	2	(BL17T)
DIL Socket 14-Pin	5	(BL18U)
DIL Socket 16-Pin	2	(BL19V)
DIL Socket 18-Pin	1	(HQ76H)
Connectector 124	1	(FL86G)
Edge Conn. End Bkt.	2	(YR58N)
Bolt 6BA x 1/2in.	1 Pkt	(3F06G)
Nut 6BA	1 Pkt	(3F18U)
Transformer 12V 1A	1	(WB25C)

A kit of parts is available for this project:

Order As **LIK95D (Digitiser Kit) Price £41.95**

The following item included in the above kit list is also available separately, but is not shown in the 1986 catalogue:

Digitiser PCB Order As **GD02C Price £11.95**

ously, adjustment of RV1 will vary the aspect ratio to suit the graphics mode of the host computer.

The digitised pictures could be stored on an 'album' disk or used as backgrounds, for games for example. Some animation may be possible, if the host computer allows screen paging, by flipping between several stored images with slightly different subject positions.

However the stored images are used, this Digitiser provides a novel and interesting use for the home computer when the games begin to pall, and an answer to that recurrent question: 'What can you do with a computer?'

Controller

This is an optional extension of the Video Digitiser, which greatly simplifies the programming required to use it. Using the Controller, software detection of Frame and Line Sync pulses is no longer necessary, this being handled solely by hardware. In operation, a start pulse is sent to the controller board and the busy line is monitored until it goes low. This indicates that a column of data has been stored which is read by the host computer, using the step input to scan through the stored information. A new position byte is sent to the Digitiser and the process repeated until the whole picture has been stored.

Circuit Description

In Figure 4, upon receipt of a start pulse at CLK of IC3a via OR gate IC7c and C4/R15, a pulse length limiting network, the Q output of IC3a goes high, gating Line Sync pulses to LSO (Line Sync Out) which is connected to the sample pulse generating circuit on the Digitiser board. IC3a Q output also gates Frame Sync to IC3b via OR gate IC7a, causing IC3b Q output to go high upon receipt of the next Frame Sync pulse (start of picture). This holds line counter (IC4) reset via OR gate IC7d, while the Q output of IC3b enables counter IC1, a

presetable counter that counts a number of 'wasted' lines before carrying, i.e. sets vertical start position of digitised picture. Note, this number should not be set (Dipswitch) higher than 55.

The carry pulse from IC1 is inverted and clocks IC3b, resetting it, via IC7a. IC1 is disabled by Q output of IC3b going high and IC4 enabled by Q going low. IC2 was clocked by Frame Sync via IC7.5 and its Q output gates CHIP SELECT pulses from IC8 through to clock input of IC4. These CHIP SELECT pulses are derived from the end of conversion output of the Digitiser board, as are WRITE ENABLE and ENABLE for the RAM and RAM Buffer, respectively.

WRITE ENABLE comes from pulse shaping circuit C1/R10 via IC6 and the longer ENABLE pulse from C2/R11 via IC6. CS and E are exclusively OR'ed by IC8 to produce CS. Using this method to produce CS ensures that no conflict is possible on the Data Bus D0-D7 between the RAM and the Buffer (IC10/11 and IC9), since CS can only be low (active)

when either:-

- WE and E are both low. (Buffer has control of Bus) or,
- WE and E are both high. (RAM has control of Bus).

Under the control of these signals, the data from the Digitiser is passed via buffer IC9 to RAM (IC10/11 for eight bit resolution) and the line counter (IC4) advanced to the next line address. This process continues for each line until IC4 carries, resetting itself via IC6/7 and resetting IC3a via IC7c. Line and Frame Sync pulses are no longer gated to the counters/flip-flops and the busy line goes low, indicating that a vertical column of screen data has been stored in the controller RAM, and is ready to be transferred to the host computer.

The 'step' input is now enabled by the Q output of IC3a and data may be transferred by reading the Data Bus and applying a step pulse, which clocks IC4, stepping it to the next line address, until all data has been read (≤ 256 lines depending on system requirement).

Listing 1.

```

5 GRAPHICS 9
10 REM . * SET UP PORTS *
20 POKE 54019,56
30 POKE 54017,255
40 POKE 54019,60
50 POKE 54018,56
60 POKE 54016,112
70 POKE 54018,60
80 C=0
100 PA=54016:PB=54017
200 POKE PB,230
250 POKE PA,64:POKE PA,0
300 IF PEEK(PA)/128>=1 THEN GOTO 300
400 FOR X=0 TO 191:LUM=PEEK(PA)
410 GOSUB 2000:POKE PA,32
420 POKE PA,0:NEXT X
430 C=C+1:POKE PB,230-C
500 GOTO 250
2000 IF C=80 THEN GOTO 2000
2010 COLOR LUM:PLOT C,X:RETURN

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DIGITISER CONTROLLER PARTS LIST

RESISTORS: All 0.6W 1% Metal Film

R1-9 10k
R10,11 22k
R12 4k7
R13,14,15 100k

CAPACITORS

C1 470pF Ceramic
C2 1uF Poly Layer
C3 220nF Poly Layer
C4 4u7F Poly Layer
C5-15 100nF Minitdisc

SEMICONDUCTORS

D1-4 1N4148
IC1 40103BE
IC2,3 4013BE
IC4 4040BE
IC5 4081BE

IC6 74HC14
IC7 4071BE
IC8 4070BE
IC9 74LS244
IC10,11 2114

9 (M10K)
2 (M22K)
1 (M4K7)
3 (M100K)

MISCELLANEOUS

Digitiser Controller PCB
DIL Switch SPST (Octal)
Connector 132

Edge Conn. End Bkt.
DIL Socket 18-Pin
DIL Socket 20-Pin
DIL Socket 14-Pin
DIL Socket 16-Pin

(UB10L)
(QW43W)
(OX26D)
(QQ86L)
(QW12N)

(GD03D)
(XX27E)
(FL86T)
(YR88N)
(HO77H)
(HO77H)
(BL18U)
(BL19V)

A kit of parts is available for this project:

Order As LK96E (Digitiser Controller Kit) Price £29.95
The following item included in the above kit list is also available separately, but is not shown in the 1986 catalogue:
Digitiser Controller PCB Order As GD03D Price £11.95

Construction

Locate and solder all resistors, capacitors and diodes, noting polarities. Fit and solder Dipswitch and all IC sockets, locating Dipswitch with the writing on its side facing the edge of the board, and the polarity notches of the IC sockets matching the square block marked on each IC legend. See Figure 5. Carefully insert all IC's in their respective positions, taking note of correct orientation. Wire the edge connector as shown in Figure 6, referring to your computer manual or instructions for your I/O port, where applicable. Keep all wiring between the boards and the computer as short as possible to avoid corruption of data. Take care to check all joints/connections for short circuits, dry joints, etc.

Testing

Plug both boards into their edge connectors and apply power. Check the



5V supply using a multimeter. IC3 pins 1 and 13, IC2 pin 1 should all be low (<1V), relative to 0V. All being well, switch off and connect the circuits to the host computer and video source as shown in Figure 6.

Programming

Listing 1 shows a BASIC language program to operate the Digitiser. The

addresses given relate to the port addresses of the Atari 400/800 computers. A BASIC program will take several minutes to complete the screen display, but has the advantage of being very quick and easy to write. For those who desire faster operation, a machine code program will be required. An example (Listing 2) is provided in 6502 assembly language, again for the Atari 400/800 computers, although no explanation of this program will be included here, this being beyond the scope of the present article.

Throughout this article, it has been assumed that the reader has a basic understanding of the construction of a video signal. For those who wish to gain some knowledge on the subject, the following book is recommended:

Questions and Answers on Video by Steve Money, available from Maplin (Stock Code WC77J).

Listing 2.

```

10 *=$7000
20 PORTA=$D300
30 PORTB=$D301
40 PACTL=$D302
50 PBCTL=$D303
60 NMIIEN=$D40E
70 IRGEN=$D20E
80 POKMSK=$0010
90 DMACTL=$D400
0100 SDMCTL=$022F
0110 SAVMC=$0058
0120 MASK=$06F9
0130 LINES=$06FA
0140 POSIT=$06FB
0150 SCNCOL=$06FC
0160 OFFSET=$00D4
0170 FINCOL=$06FE
0180 PLA
0190 INIT LDA #00
0200 STA LINES
0210 LDA #240
0220 STA POSIT
0230 LDA SAVMC
0240 STA SCNCOL
0250 LDA SAVMC+1
0260 STA SCNCOL+1
0270 CLC
0280 CLD
0290 TAX
0300 LDA SCNCOL
0310 ADC #40
0320 STA FINCOL
0330 BCC NOINT
0340 INX
0350 NOINT STX FINCOL+1
0360 LDA#38
0370 STA PBCTL
0380 STA PACTL
0390 LDA#96
0400 STA PORTA
0410 LDA#FF
0420 STA PORTB
0430 LDA#3C
0440 STA PBCTL
0450 STA PACTL
0460 START LDA SCNCOL
0470 STA OFFSET
0480 LDA SCNCOL+1
0490 STA OFFSET+1
0500 LDA POSIT

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0510 TOG STA PORTB
0520 LDA#64
0530 STA PORTA
0540 JSR DELAY
0580 LDA#0
0590 STA PORTA
0600 BIT PORTA
0610 BMI HI
0620 GETLLM LDX PORTA
0630 LDA POSIT
0640 LSR A
0650 LSR A
0660 BCC MULT
0662 TXA
0664 LDX#240
0666 STX MASK
0670 AND #0F
0680 JMP STORE
0690 MULT TXA
0692 LDX#15
0694 STX MASK
0700 ASL A
0710 ASL A
0720 ASL A
0730 ASL A
0750 STORE LDY#00
0760 DRA (OFFSET),Y
0762 LDY#40
0764 LDA(OFFSET),Y
0766 AND MASK
0770 NEWROW STA(OFFSET),Y
0780 CLC
0790 CLD
0800 LDA OFFSET
0810 ADC #40
0820 STA OFFSET
0830 BCC LNCHK
0840 CLC
0850 INC OFFSET+1
0860 LNCHK INC LINES
0870 CMP #191
0880 BCC STEP
0890 LDA #00
0900 ODD LDA LINES
0910 LDA POSIT
0925 LSR A
0930 BCC PICFIN
0940

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0950 LDA SCNCOL
0960 ADC #01
0970 STA SCNCOL
0980 BCC PICFIN
0990 INC SCNCOL+1
1000 DEC POSIT
1005 LDA SCNCOL
1020 CMP FINCOL
1030 BCC NEWCOL
1040 LDA SCNCOL+1
1050 CMP FINCOL+1
1060 BCC NEWCOL
1070 FIN RTS
1080 STEP LDA#32
1090 STA PORTA
1100 JSR DELAY
1110 LDA#0
1160 STA PORTA
1170 JMP GETLLM
1180 LDA#16
1190 STA POSIT
1200 LDA SAVMC+1
1210 LDA SCNCOL+1
1220 LDA SAVMC
1230 CLC
1240 ADC #40
1250 STA SCNCOL
1260 BCC NEWCOL
1270 INC SCNCOL+1
1280 NEWCOL JMP START
1290 DIS LDA #00
1300 STA IRGEN
1310 STA POKMSK
1320 STA NMIIEN
1330 STA DMACTL
1340 STA SDMCTL
1350 RTS
1360 ENA LDA #C0
1370 STA IRGEN
1380 STA POKMSK
1390 STA NMIIEN
1400 LDA #34
1410 STA DMACTL
1420 STA SDMCTL
1430 RTS
1440 DELAY LDX#30
1450 DOWN DEX
1460 BNE DOWN
1470 RTS

```